

PROCESS FOR ETCHING VIAS IN ORGANOSILICATE GLASS
MATERIALS WITHOUT CAUSING RIE LAG

Abstract of the Disclosure

Process for etching features in wafers incorporating OSG dielectrics. The
5 process results at once in minimal RIE lag, minimal bowing of the features formed by
the etch process, good etch profiles, good resist selectivity, and good etch uniformity
across the wafer. In order to provide these desirable results, a novel etch gas mixture,
including CH₂F₂ and CF₄ is employed. According to one embodiment of the present
invention, this novel gas mixture is employed as part of a three-step etch process
10 wherein the several etch steps have varying degrees of etch selectivity between wafer
components.

The methodology of the present invention is capable of implementation on a
wide variety of existing semiconductor etch equipment.

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